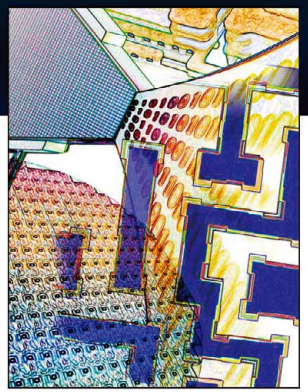
Circuit Reliability Success Story: HiSilicon usage of Calibre PERC

HiSilicon / Mentor Graphics

ABSTRACT

At advanced nodes, increased interactions and local effects make circuit reliability verification progressively more complex. Designers need checking strategies that expand beyond traditional verification and simulation techniques. TSMC and Mentor Graphics collaborated to develop extensive checks for Electrostatic Discharge and Latch-Up (ESD/LUP). These checks, which are implemented with the Calibre PERC reliability tool, help designers identify and eliminate these causes of electrical failure quickly and accurately. HiSilicon incorporated these techniques beginning with the 28nm node, and has expanded their use at every new process node, with development continuing for N7. We describe the overall offering, and HiSilicon's experience with those checks for their most advanced designs.

Circuit Reliability Success Story: HiSilicon usage of Calibre PERC



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TSMC OIP, September 2016

Calibre PERC HISILICON Mentor Graphics

Mission Profiles – Different Applications

- High reliability has become a focus for all application areas
  - How high?
  - How rigorous does verification need to be?
- How are your ICs being used in the system?
  - Functional safety (need ISO 26262)
  - Infotainment, consumer, others
  - Does expected use, match actual use?
- What is the cost of failure?
  - Don't want to own the IC design that fails
- Need to Leverage best in class IC verification solutions
  - For both you and your suppliers

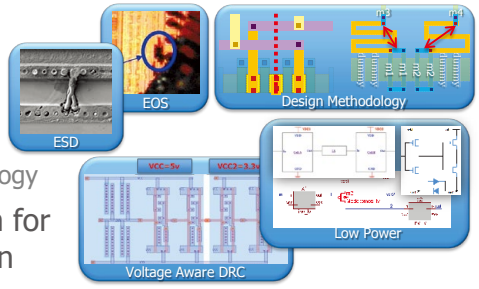

Transportation / Medical


Mobile / Wireless


General CPU / Server Farms

Calibre PERC – A Reliability Verification Platform

- Calibre PERC – Industry's reliability verification solution
  - Unique solution which considers the design context
  - Verification beyond "Traditional" DRC, LVS and ERC
- Not just a point tool solution
  - Provides a system view of how design elements interact
  - Used throughout the entire design flow: schematic, layout, final verification
- Typical application areas
  - ESD, EOS, Latch-up
  - Voltage-aware DRC
  - Low/Multi-power designs
  - General reliability, methodology
- Provides a robust platform for circuit reliability verification



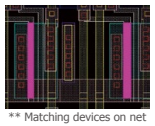
Calibre PERC
Core Capabilities – Areas of investment

- Nets and Devices
- Interconnect Robustness
- High-Level Checks
- Voltage Propagation
- Waivers
- Calibre PERC + Tcl + YS

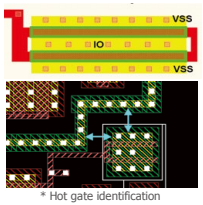
Your Own Applications

Devices, Cells and Topological Paths

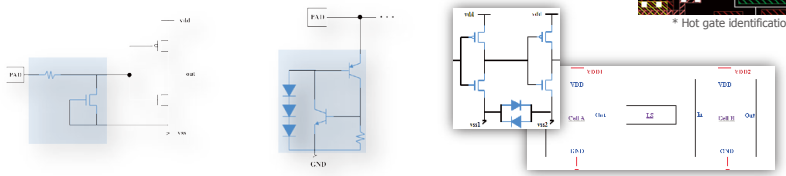
- Topological checks
  - Based on source or layout netlist (LVS extraction)
  - Can reference cell names
  - Verify signals crossing multiple power domains
  - Addresses reliability concerns / EOS
- Layout centric verification
  - Focused DRC rule checks
  - Logic Driven Layout (LDL)
- User defined checks and feedback



** Matching devices on net



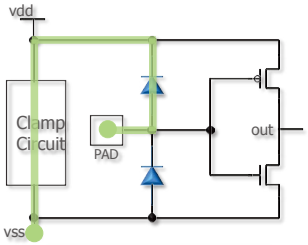
* Hot gate identification

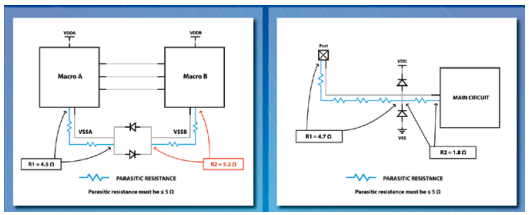


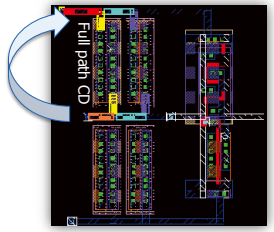
* T. Smedes, et. al., "A DRC-Based Check Tool for ESD Layout Verification", EOS/ESD 2009, pp 4A.2-1 - 4A.2-9
** P. Gibson, et. al., "A Framework for Logic-Aware Layout Analysis", ISQED 2010, pp171-175

Interconnect Robustness

- Reliability concerns on interconnect
  - Point-to-point resistance (P2P)
  - Current density (CD)
  - Electromigration (EM)
- Dynamic constraints for CD/EM
  - Allows for fine grain control and filtering of false violations

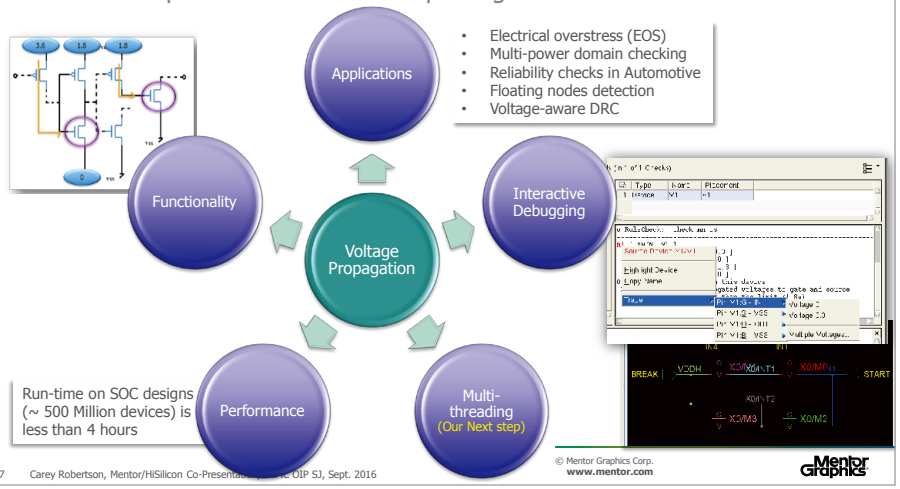






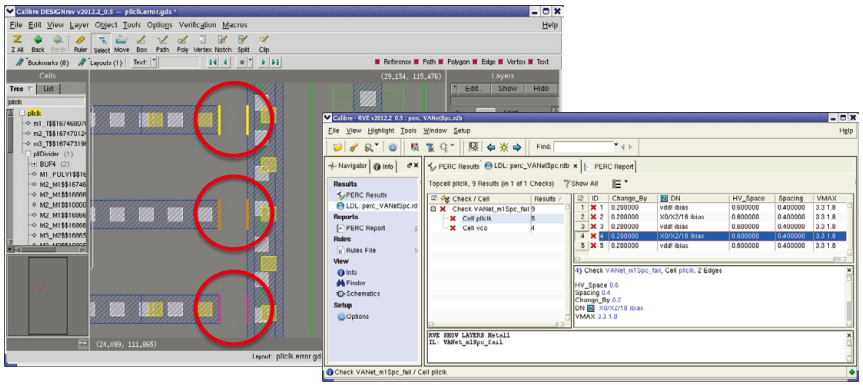
Voltage Propagation

- Efficient automated static analysis
  - Great performance on full-chip designs



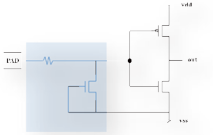
Voltage Aware DRC Debug

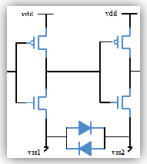
- Use existing text, or easily generate (Calibre PERC)
  - Flows without text are possible with Calibre PERC
- No complex marker layers

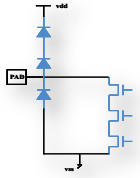


ESD

- Validate correct structures in place
- Design robustness checks
  - — Primary/secondary clamps
  - — Devices correctly sized, interconnect
- Applicable at all process nodes
  - — Focus area for many foundries





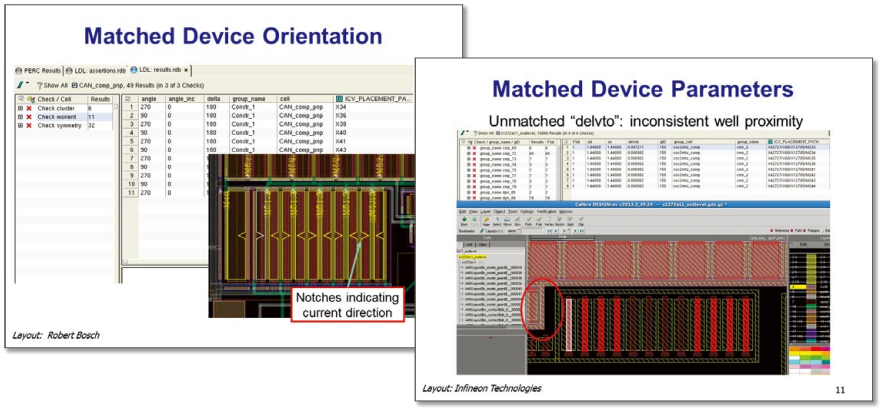


TSMC Foundry Decks for TSMC9000 IP

- Extensive collaboration to create a high reliability ecosystem
- Whole chip (system-level) verification
  - — TSMC ESD/Latch-up decks available for N28 and N20 customers
  - — N16 upon request
  - — Provides complete ESD/LUP DRM coverage
- IP level
  - — TSMC9000 support
  - — N28, N20SoC, N16FF
  - — First checks will focus on IO IPs

Analog Constraint Checking

- Subtle design errors are often difficult to identify without automation



Source: Presentation 5B-2, ASP-DAC 2015

Security Level:

HiSilicon Product Introduction

Morphy Gao
Senior Physical Design Engineer

www.huawei.com

General Overview of HiSilicon

- **Overview**
  - — HiSilicon Technologies Co., Ltd was established in October 2004;
  - — Formerly ASIC Design Center of Huawei Technologies, founded in 1991;
  - — More than 4500 employees worldwide, Headquarter in Shenzhen China, Design divisions in Beijing, Shanghai, Silicon Valley, Ottawa and Europe
- **Product Line**
  - — HiSilicon provides ASICs and solutions for communication networks and digital media
    - – Wireless Terminal
      - – Wireless Terminal Chipset Solution
      - – Application Processor Solution
    - – Wireless and Fixed Network
      - – Wireless/Fixed Networking Chipset Solutions
    - – Network Access Terminal
      - – Security and Surveillance
      - – Set Top Box
      - – DPT

Security Level:

HiSilicon ESD Design Flow and Calibre PERC Usage

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HUAWEI TECHNOLOGIES CO., LTD.

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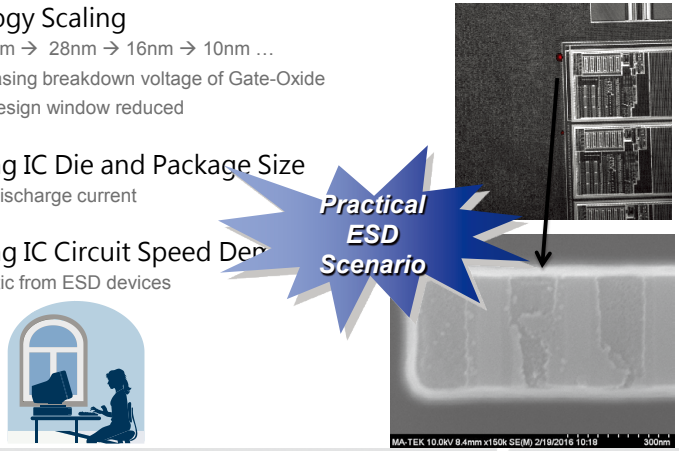
ESD Design Challenge

- How to handle ESD Protection in nano-process?
  - Technology Scaling
    - 45/40nm → 28nm → 16nm → 10nm …
    - Decreasing breakdown voltage of Gate-Oxide
    - ESD design window reduced
  - Increasing IC Die and Package Size
    - CDM discharge current
  - Increasing IC Circuit Speed Der
    - Parasitic from ESD devices



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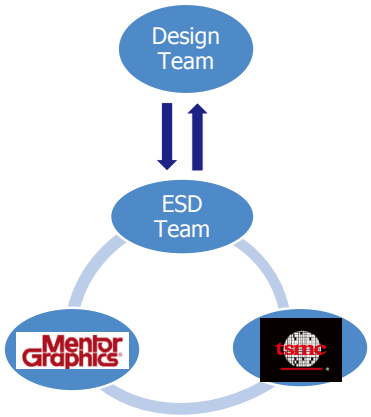
Responsibilities of Partner

- Design Team(HiSilicon)
  - ESD Design/Verification/Test/PFA requirement
- ESD Team (HiSilicon)
  - Internal consultation service
  - External contact window
  - Customized ESD Sign-off methodology
- Foundry (TSMC)
  - Process ESD solution
  - Optimized PERC decks
  - Recommendations to the technical review
- EDA Vendor (Mentor)
  - Recommendations to the Calibre PERC decks
  - Solutions that get faster with each new release



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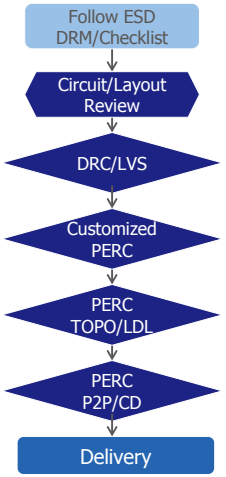
ESD Team Uses Calibre PERC as a Sign-off Tool

- Provides ESD consultation service for design team
- Support to improve the ESD quality of product
- Set up the ESD design capability for advanced process application
- Set up the ESD sign-off flow
- Develop Calibre PERC rule deck for automatic check instead of manually



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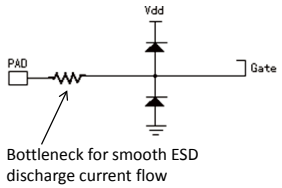
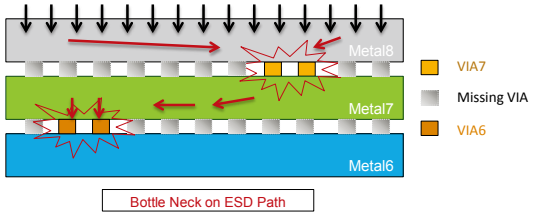
Calibre PERC for Current Density

- Checking item:



- Problem on layout:

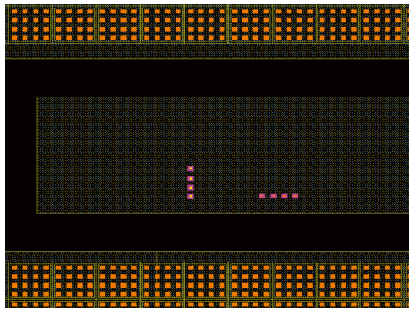


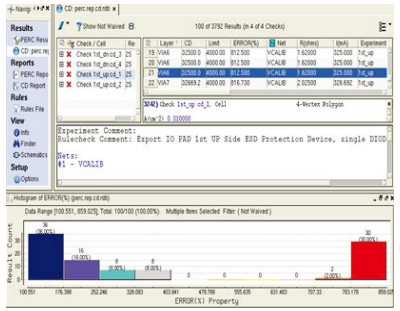
Calibre PERC for Current Density

- Case Share:

  Conductor layers on ESD discharge path must comply with ESD current density constrain

- Check Result:



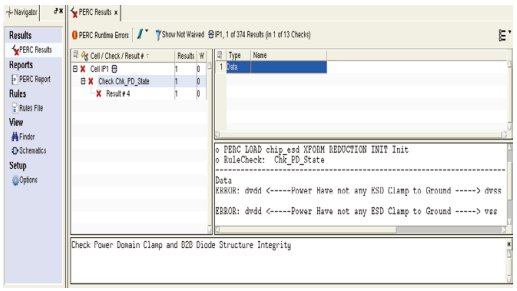


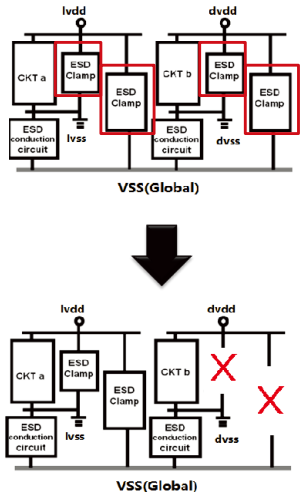
Calibre PERC for Topology

- Case Share:

  Active power clamp is required between power and ground bus

- Check Result:

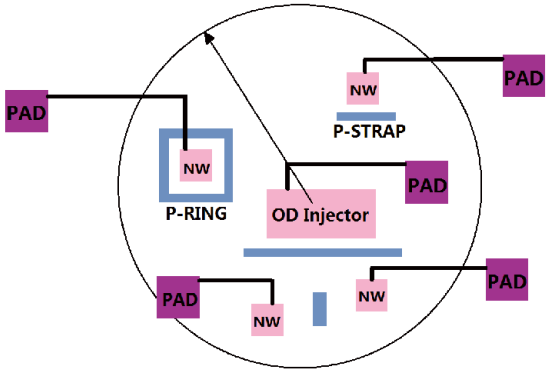




Calibre PERC for Latch-Up

- Requirement:

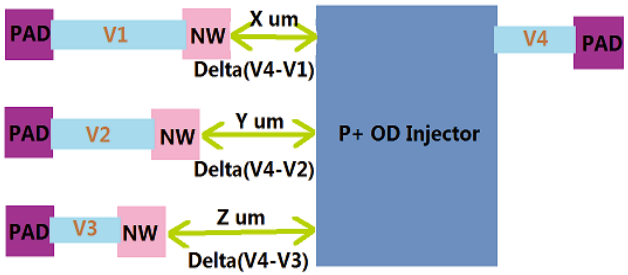
  Within 15um space from the OD injector, a NW in proximity to another NW with different potential, a PWSTRWAP is required to be inserted between these NWs.



Calibre PERC for Latch-Up

- Using Calibre PERC:

  Voltage values on NW polygons, associated net names, and spacing between different NW regions can be examined to check against Latch up trigger criteria (delta V ←→ spacing); Violated NW polygons and voltage values, spacing can be highlighted or displayed through Calibre RVE



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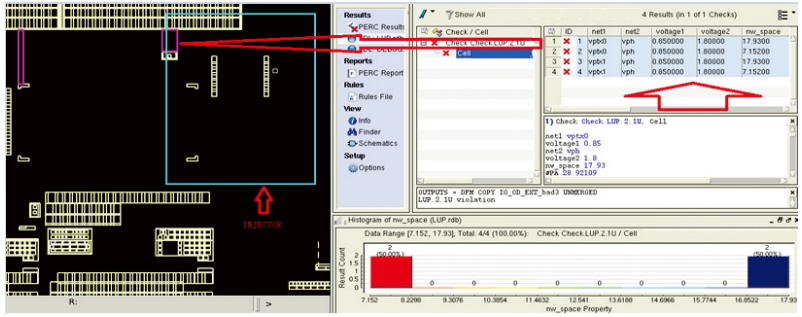
Calibre PERC for Latch-Up

- Case Share:

  Within 15um from the OD Injector , need to get two different adjacent NW voltages, Net name, NW space, and highlight the potential violation point

- Check Result:



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Thanks – TSMC & Mentor Graphics

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Thank you

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